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FIG. 1

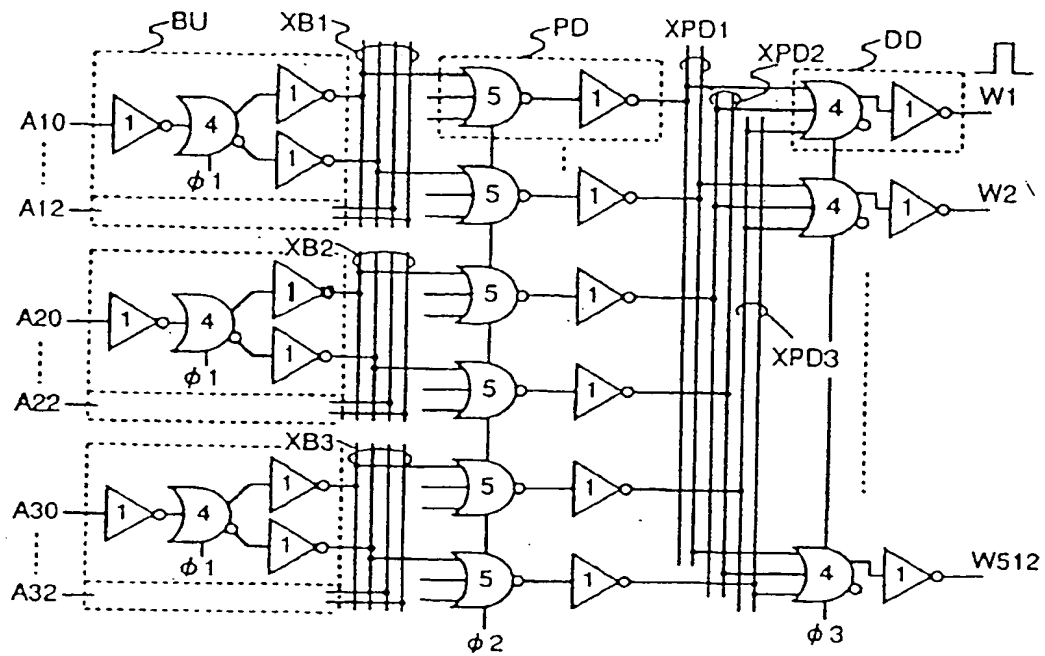


FIG. 2

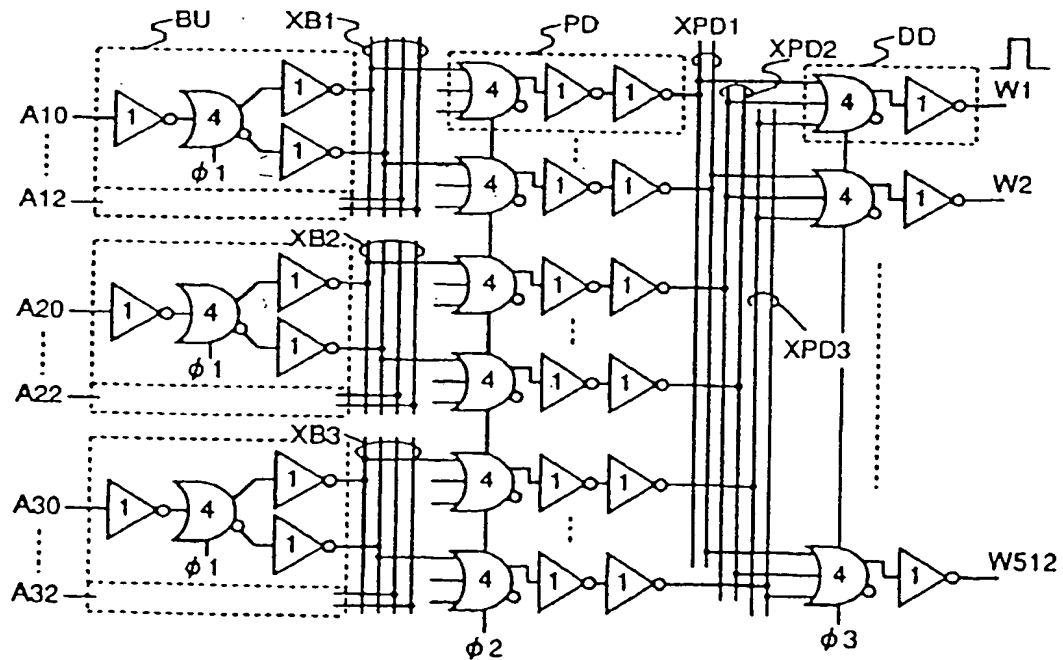


FIG. 3

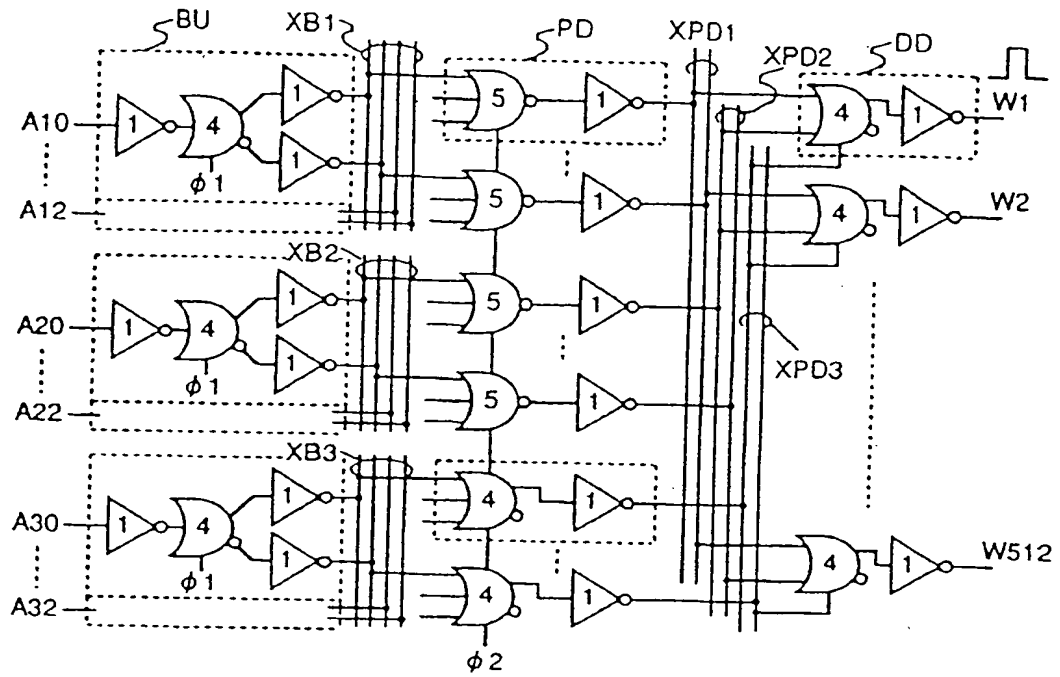


FIG. 4

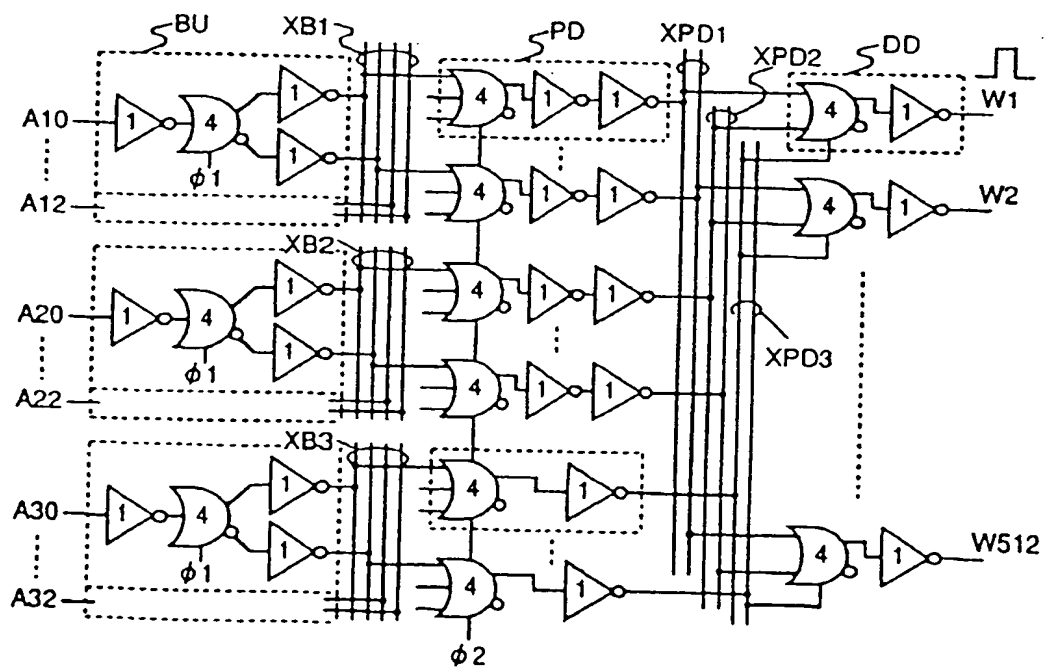


FIG. 5

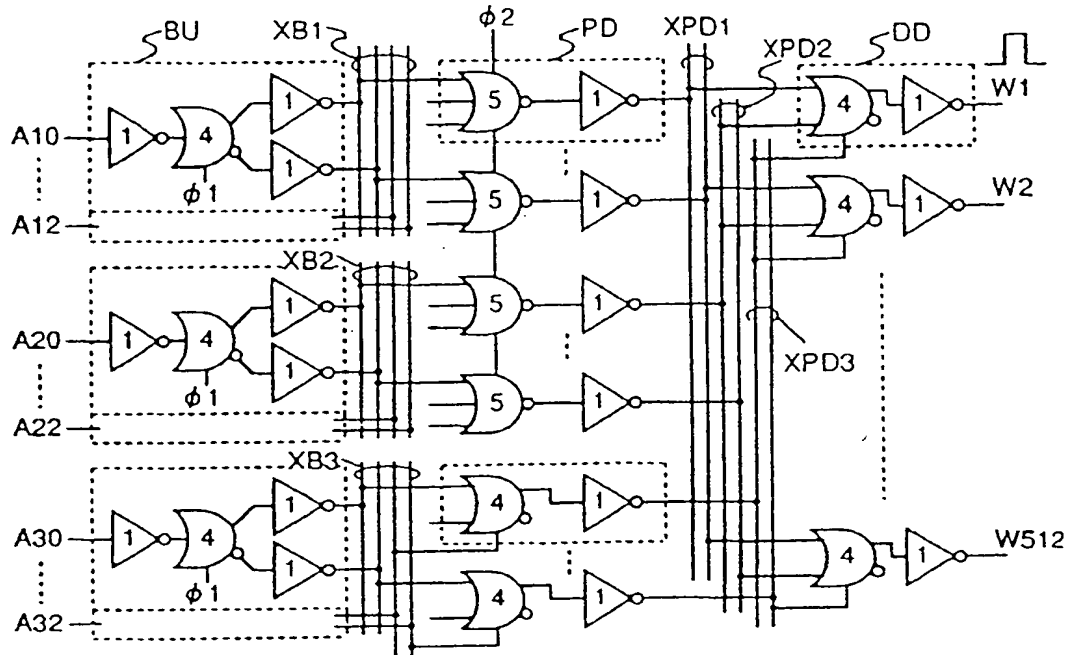


FIG. 6

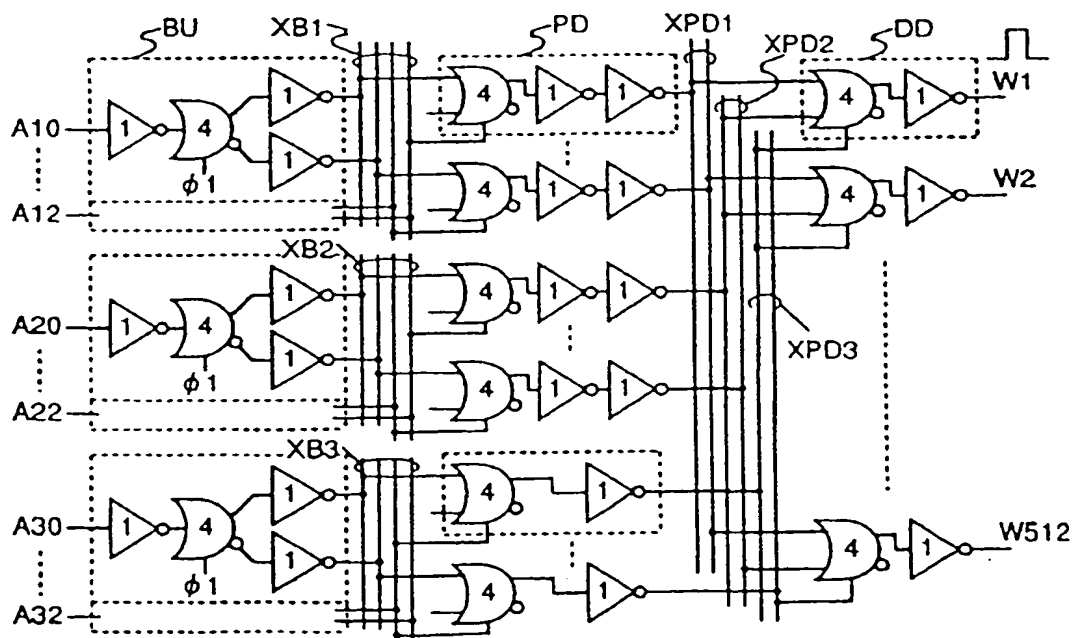


FIG. 7

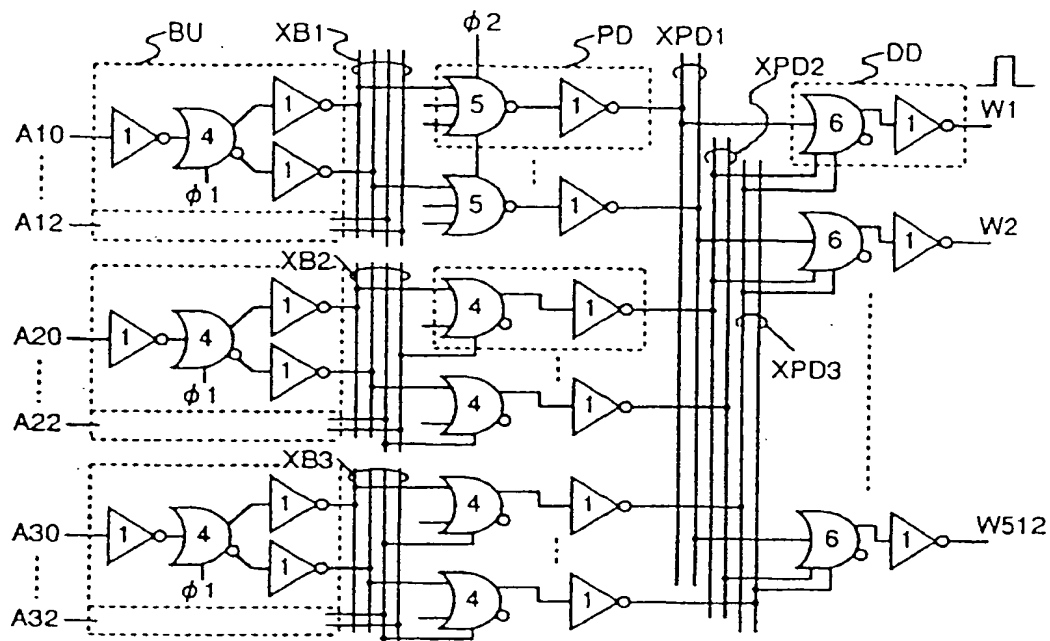


FIG. 8

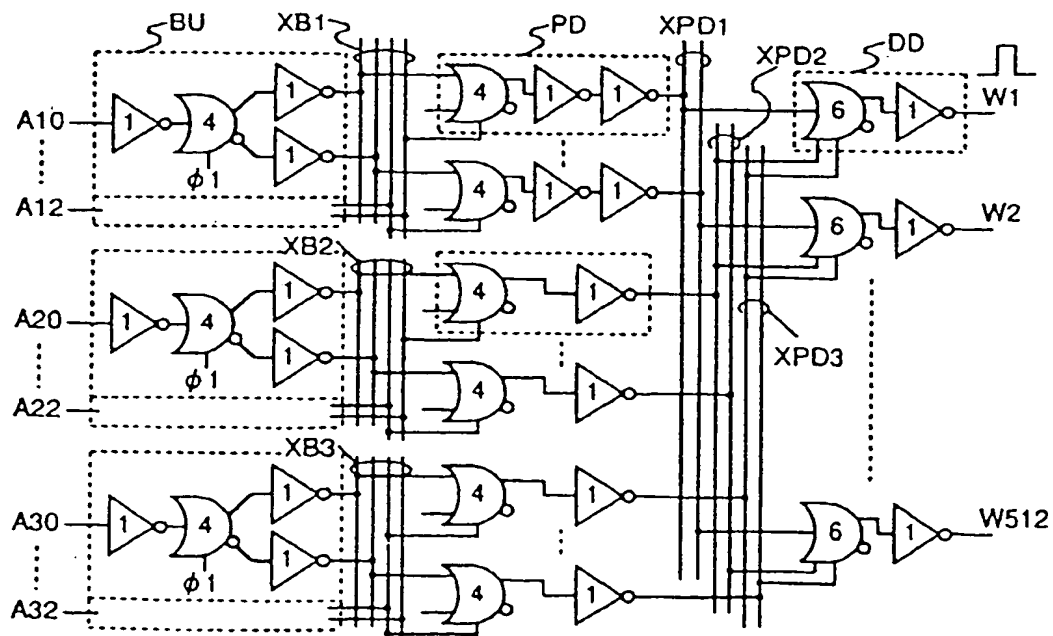


FIG. 9

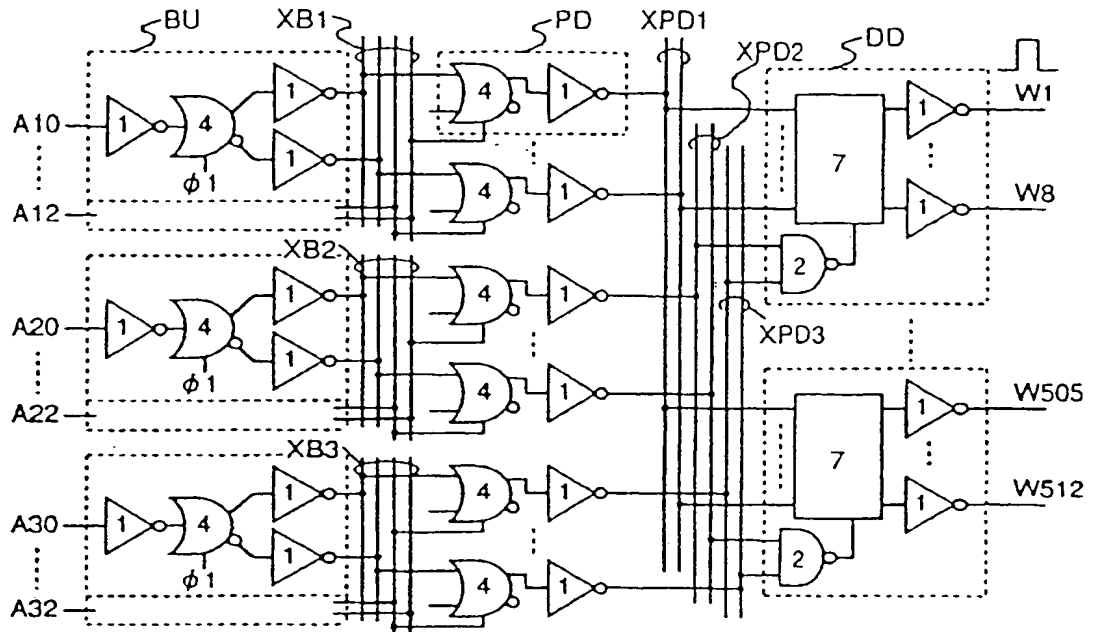


FIG. 10

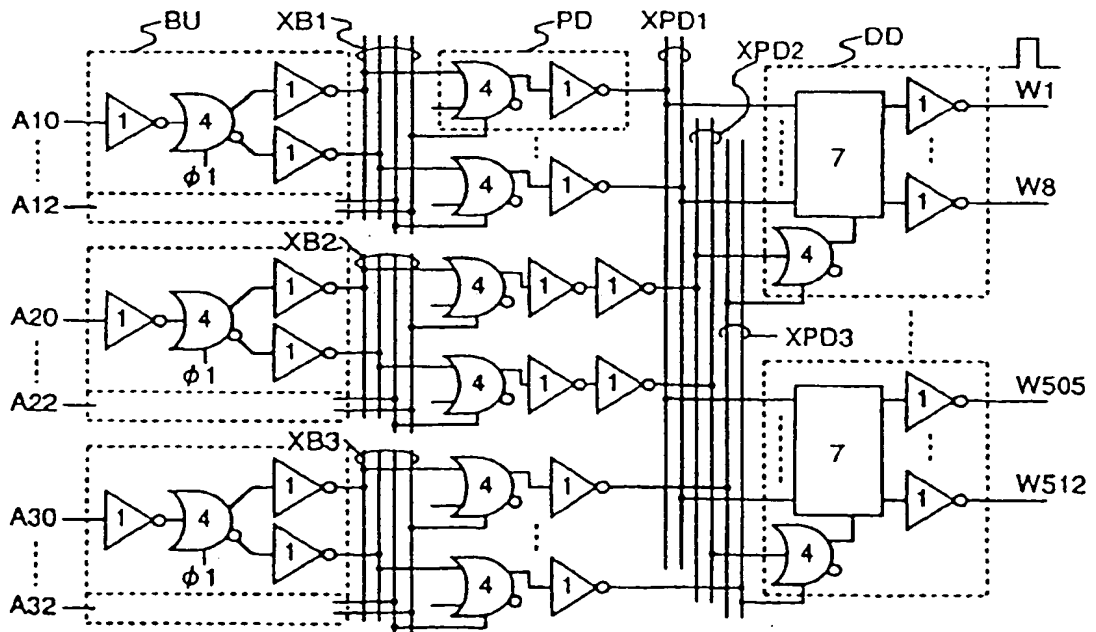


FIG. 11

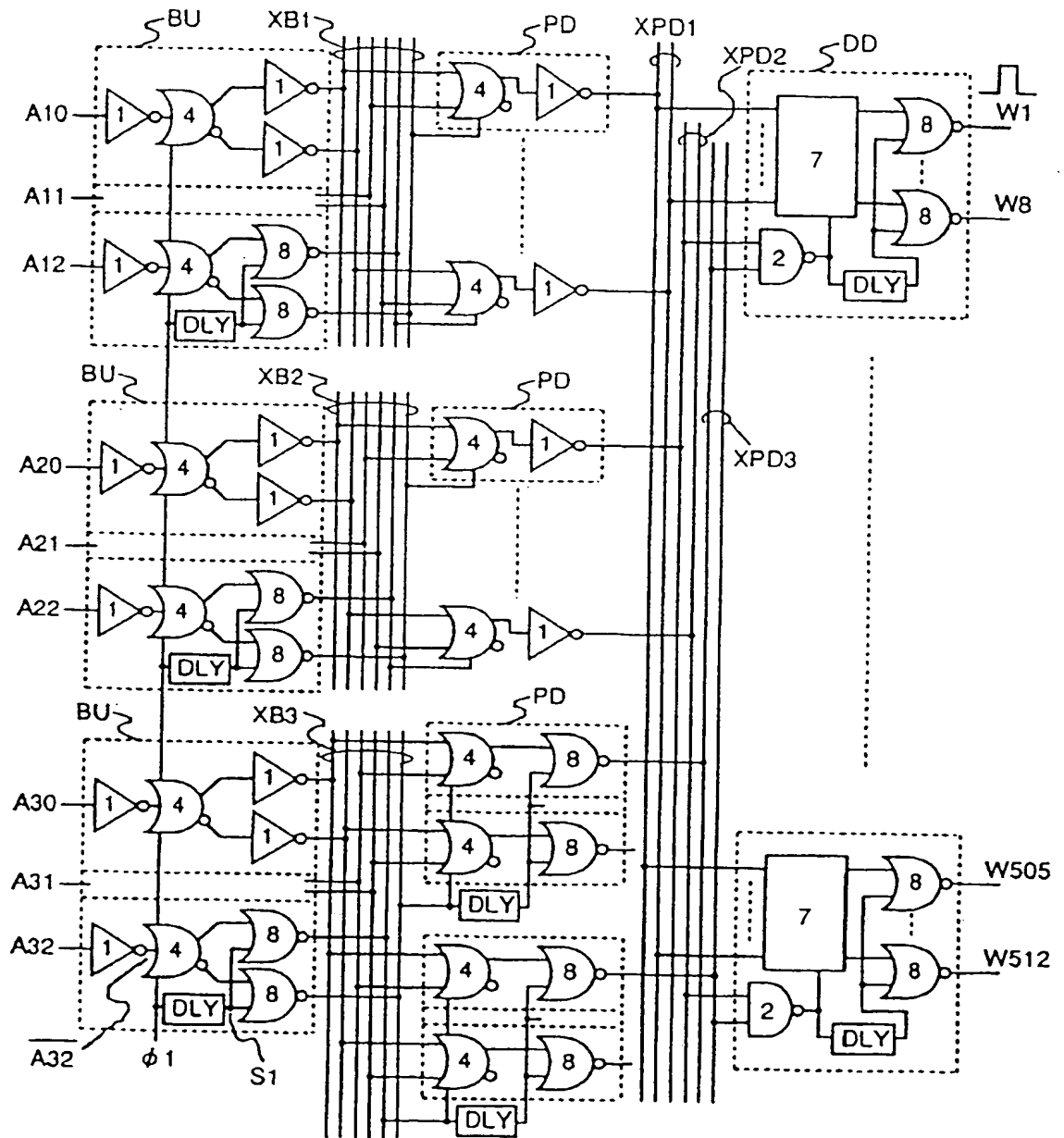


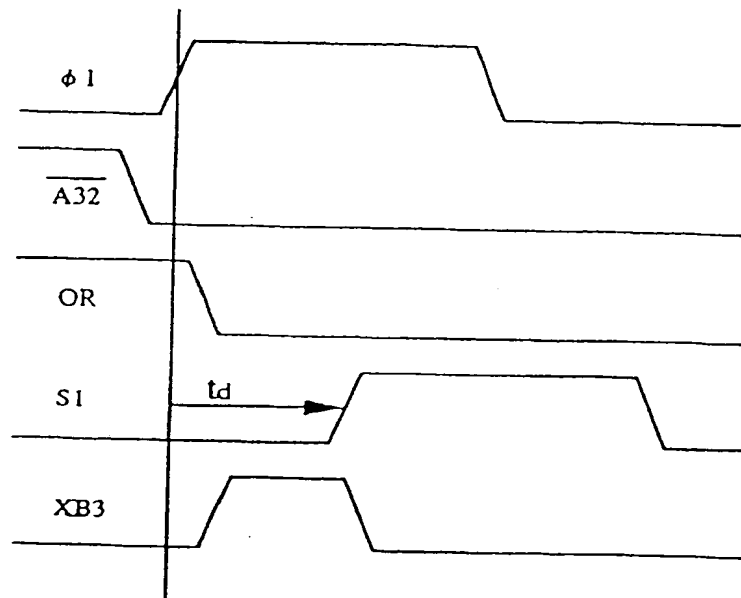
FIG. 12

FIG. 13(a)

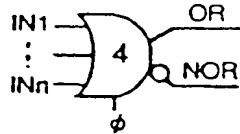
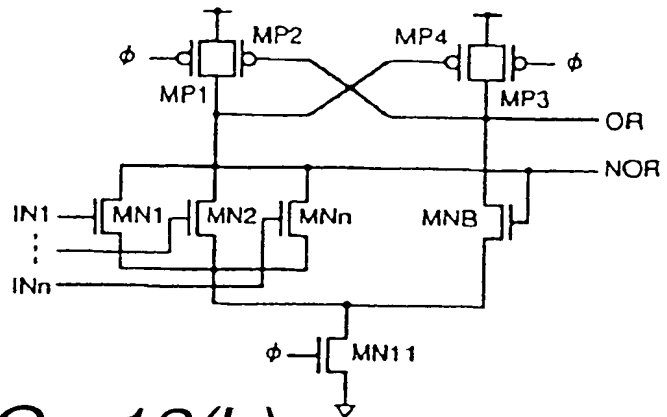


FIG. 13(b)

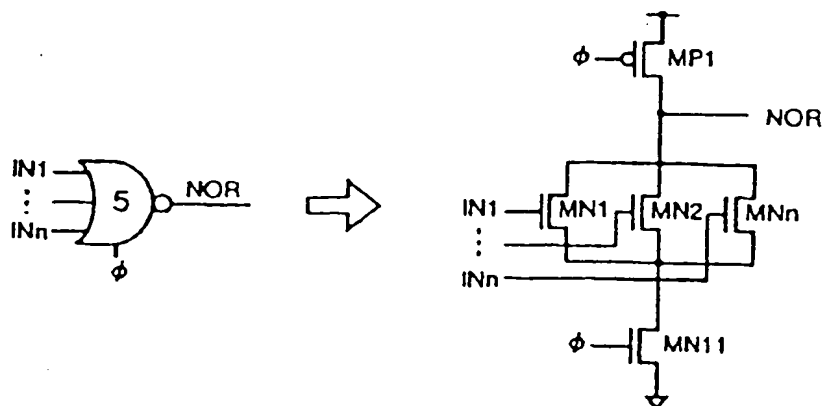
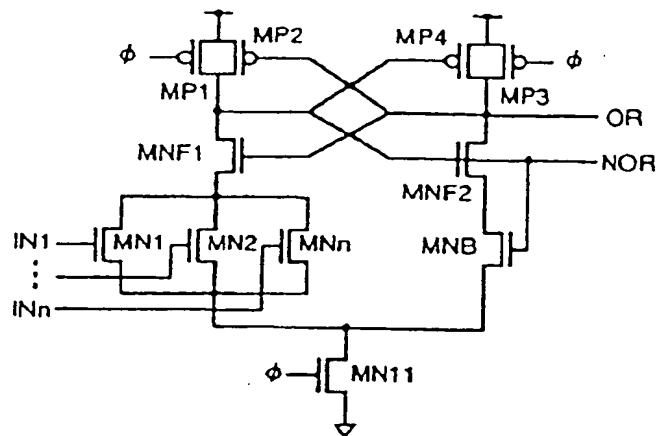


FIG. 14

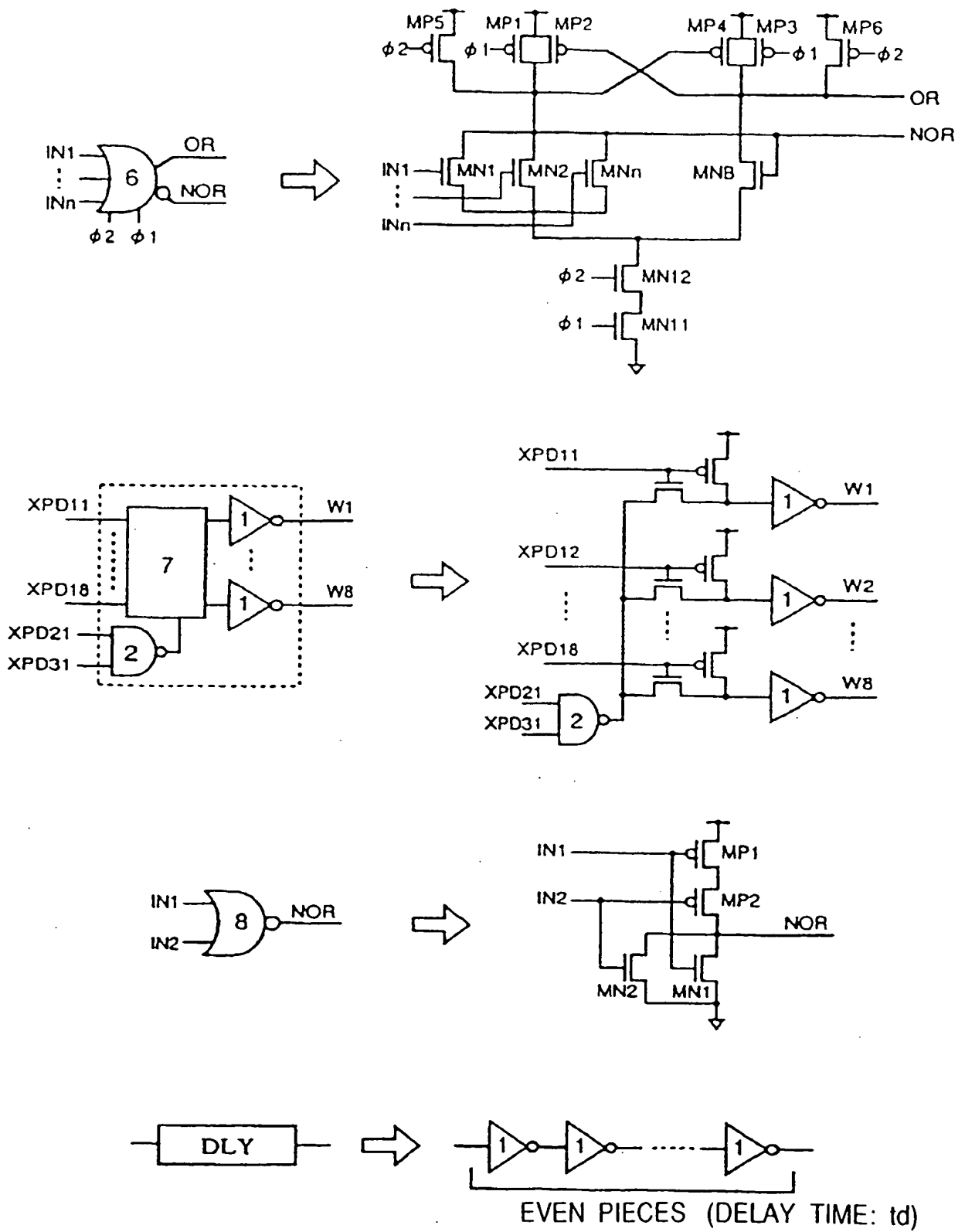


FIG. 15

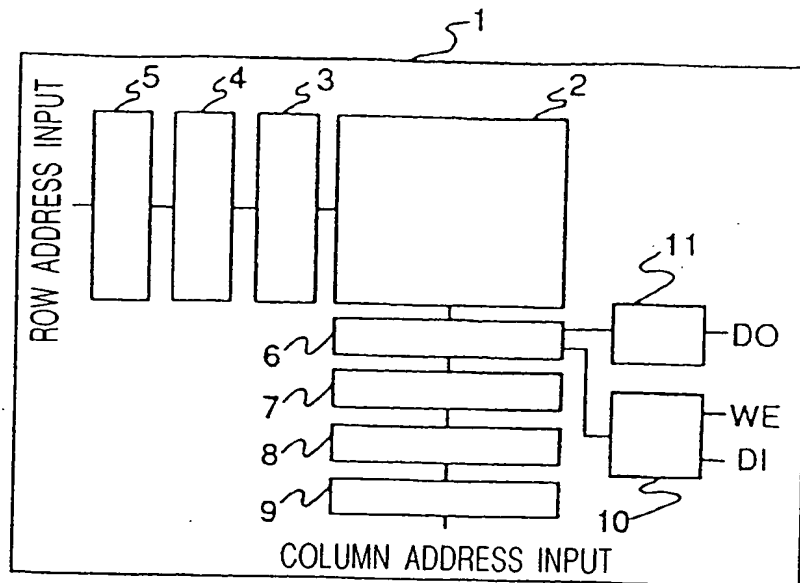


FIG. 16 PRIOR ART

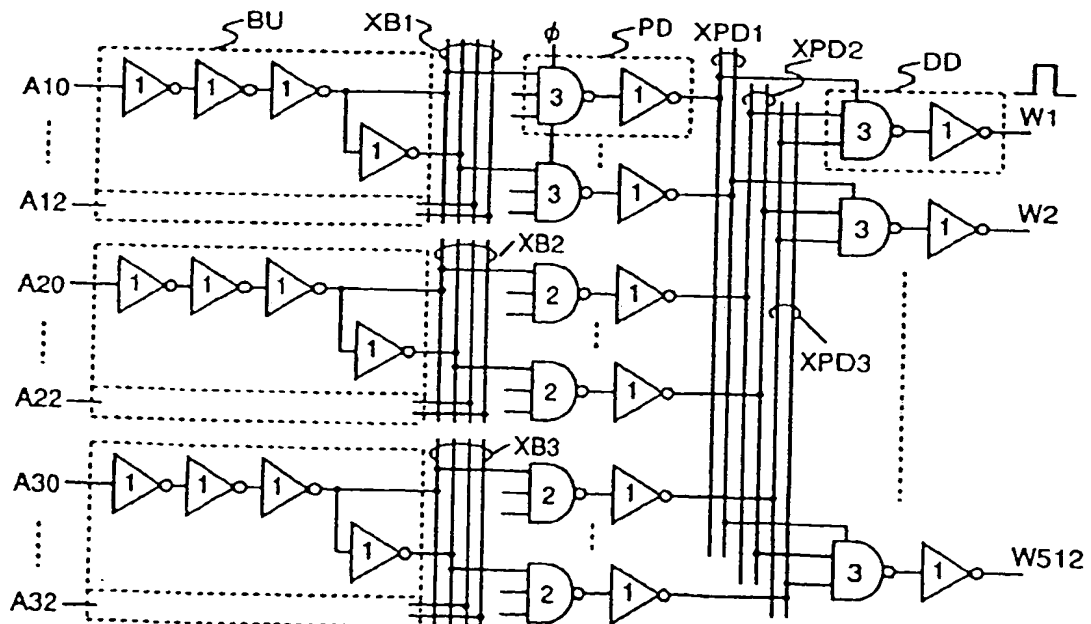


FIG. 17 PRIOR ART

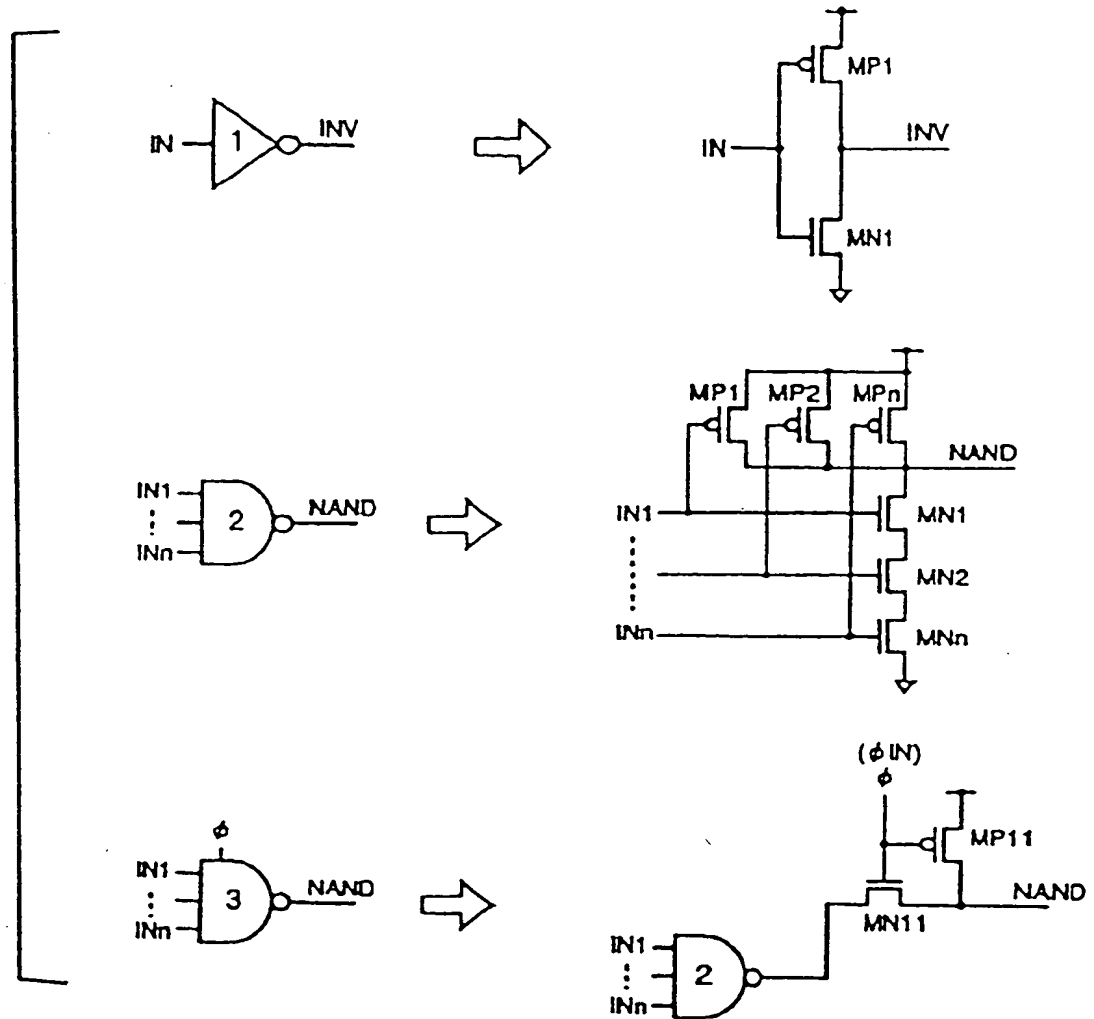
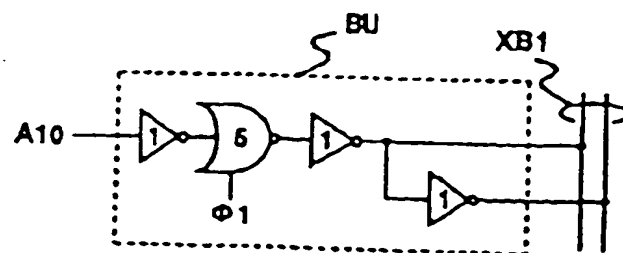


FIG. 18



[illegible]

The diagram illustrates the timing of a 1T1C CMOS inverter across three cycles: (A), (B), and (C). The signals shown are the input (IN), the clock (phi), the output (Q), and the complementary output (Q-bar). The clock phi is a square wave with a period of $t_{\phi} - t_{IN}$. The input IN is a step function. The output Q and Q-bar are shown with their respective propagation delays, t_{pd1} and t_{pd2} , and their noise margins, V_{n1} and V_{n2} . The diagram is divided into three cycles: (A) where the input is high and the output is low; (B) where the input is low and the output is high; and (C) where the input is high and the output is low. The clock phi is high during cycle (A) and low during cycle (B). The output Q is high during cycle (A) and low during cycle (B). The output Q-bar is low during cycle (A) and high during cycle (B). The diagram shows the precharge and evaluation phases of the inverter. The precharge phase occurs when the clock phi is high, and the evaluation phase occurs when the clock phi is low. The input IN is high during cycle (A) and low during cycle (B). The output Q is high during cycle (A) and low during cycle (B). The output Q-bar is low during cycle (A) and high during cycle (B). The diagram shows the propagation delay t_{pd1} from the input IN to the output Q, and the propagation delay t_{pd2} from the input IN to the output Q-bar. The noise margin V_{n1} is the difference between the output Q and the input IN during the precharge phase. The noise margin V_{n2} is the difference between the output Q-bar and the input IN during the precharge phase.

FIG. 21

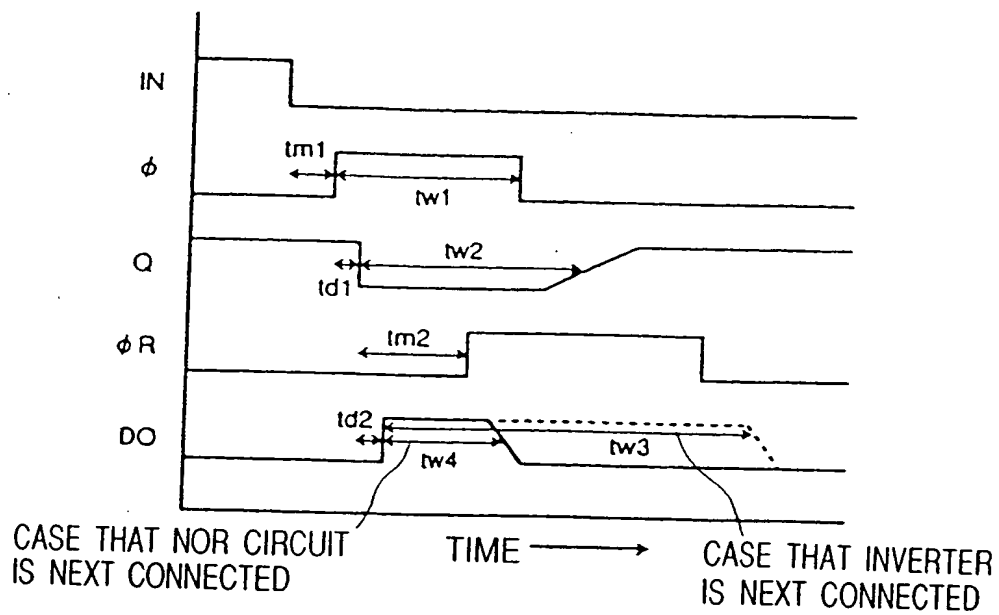


FIG. 22

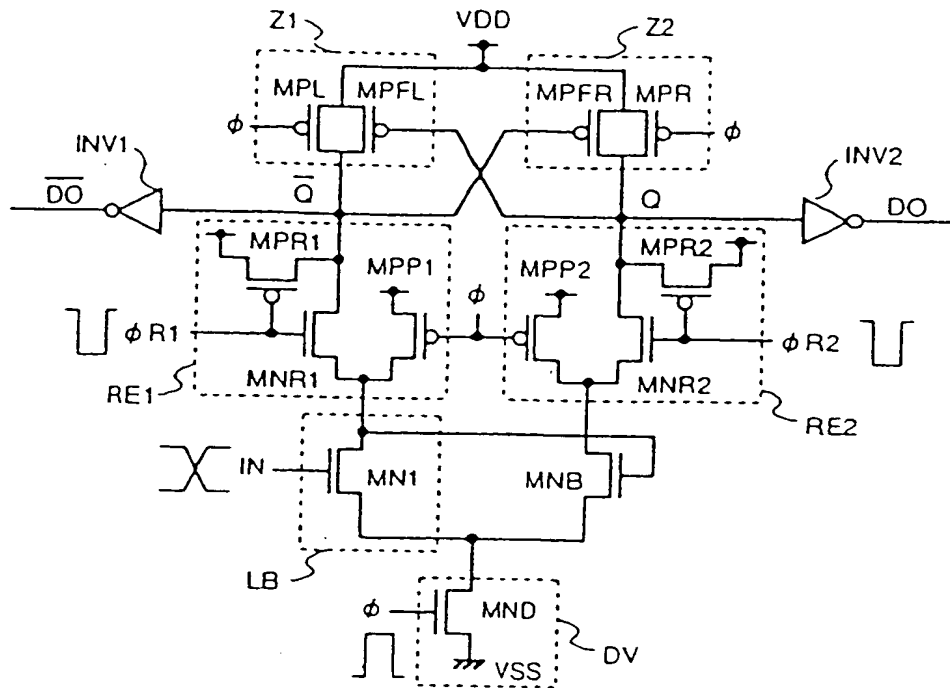


FIG. 23

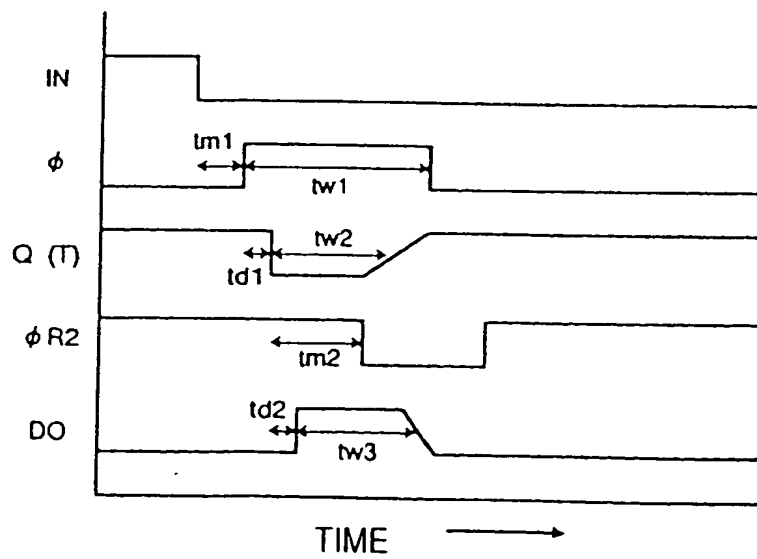


FIG. 24(a)

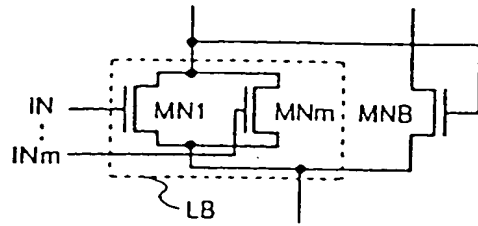


FIG. 24(b)

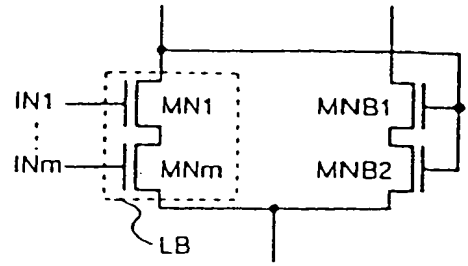


FIG. 24(c)

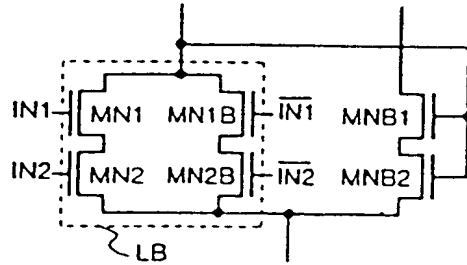


FIG. 24(d)

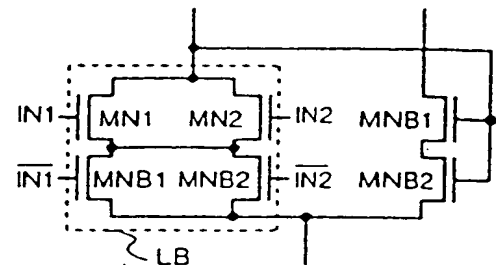


FIG. 24(e)

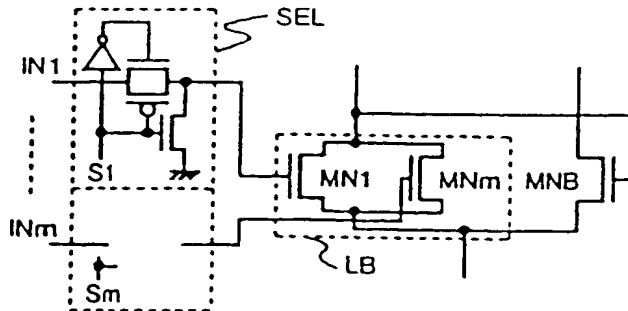


FIG. 24(f)

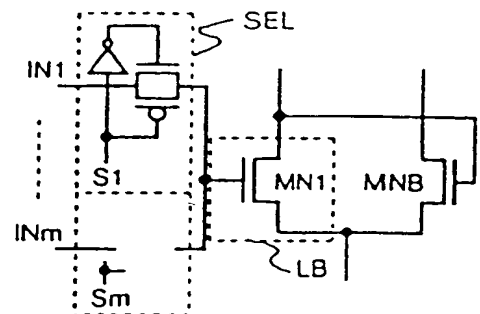


FIG. 24(g)

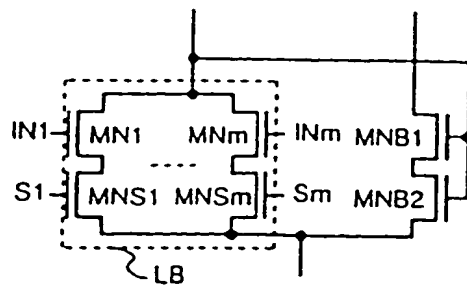


FIG. 25(a)

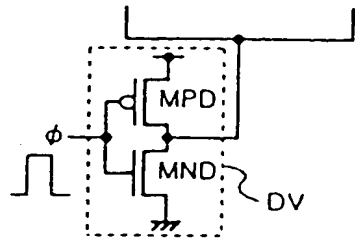


FIG. 25(b)

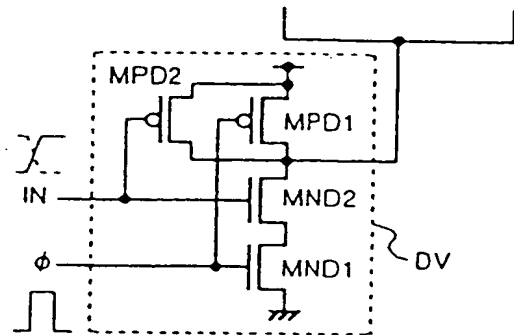


FIG. 26(a)

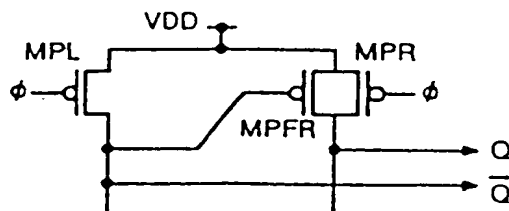


FIG. 26(b)

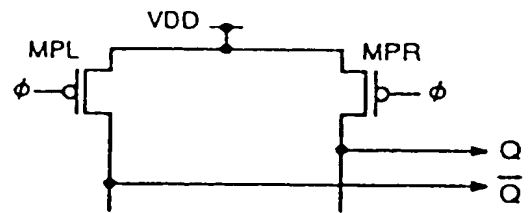


FIG. 26(c)

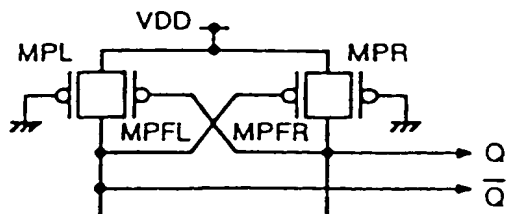


FIG. 27(a)

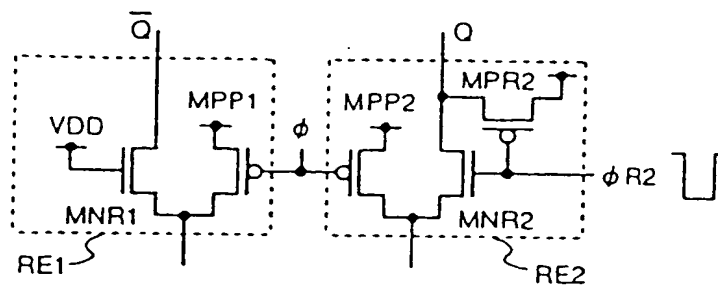


FIG. 27(b)

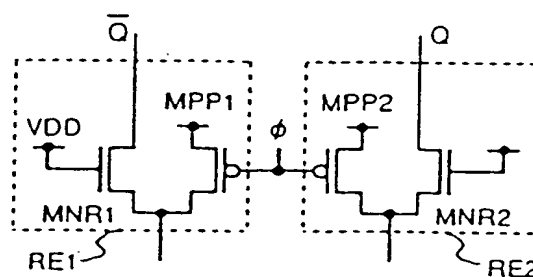


FIG. 28

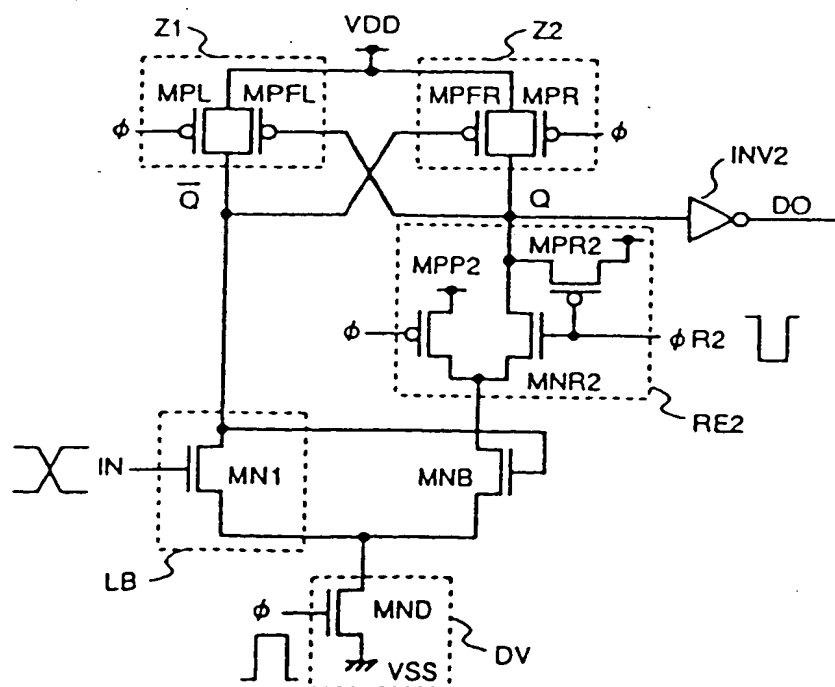


FIG. 29

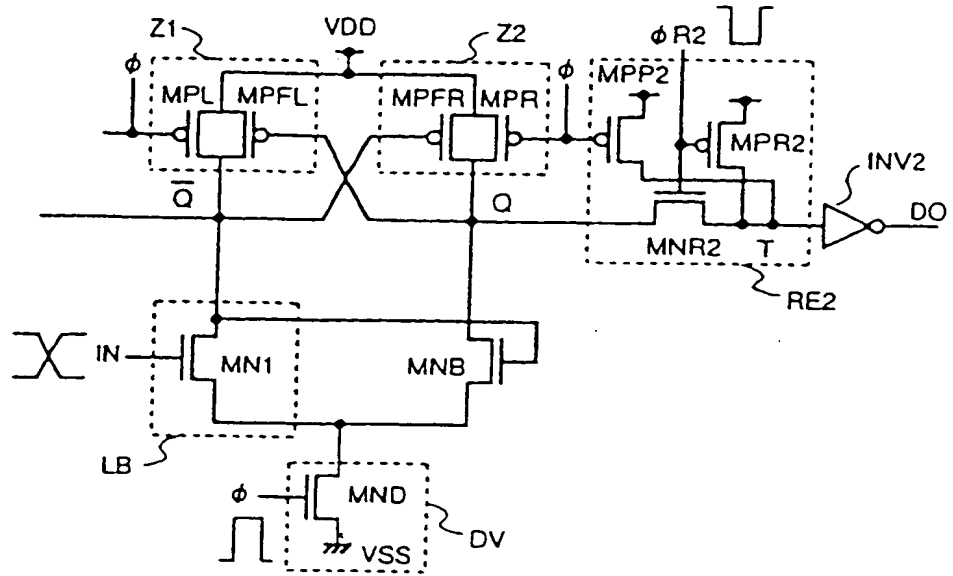


FIG. 30

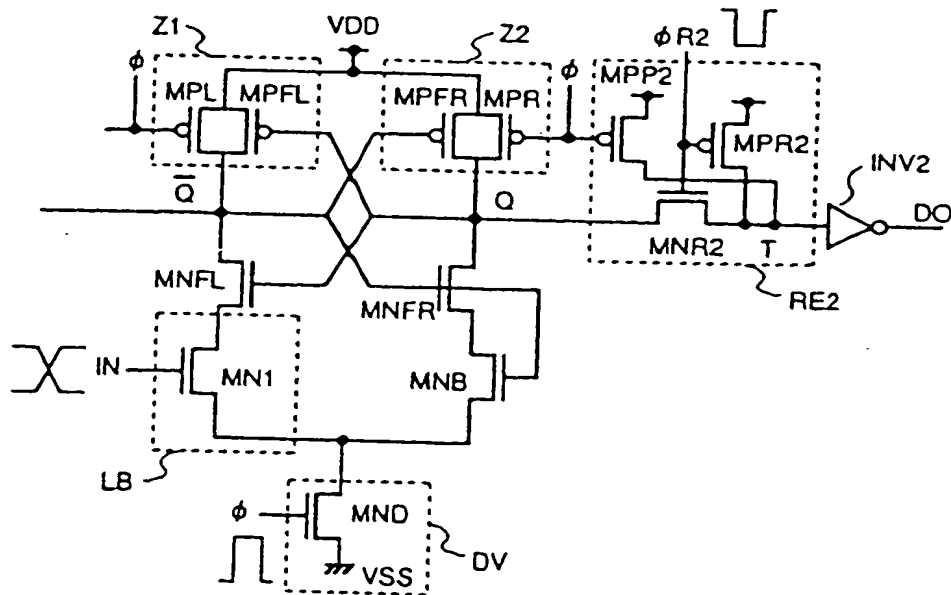


FIG. 31

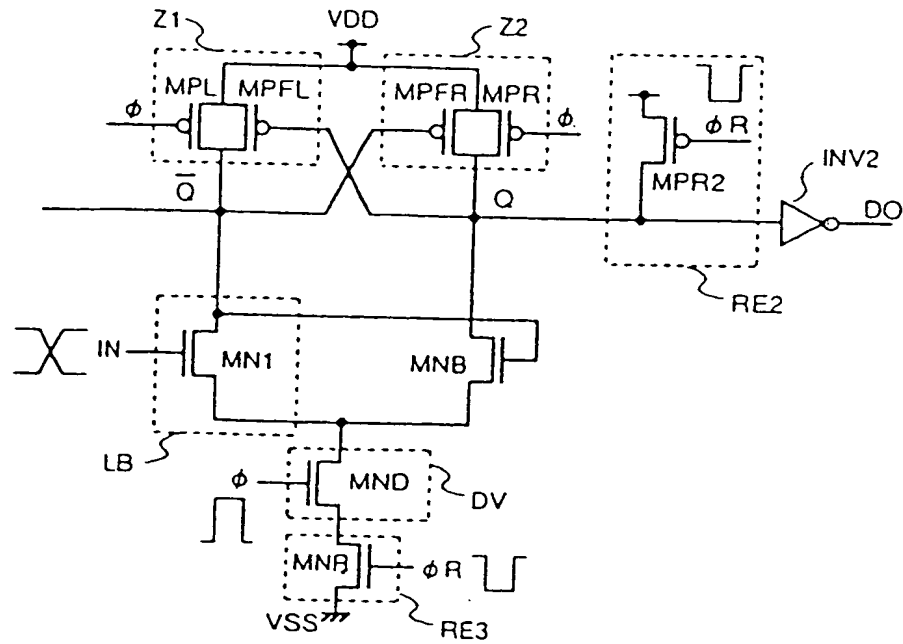


FIG. 32

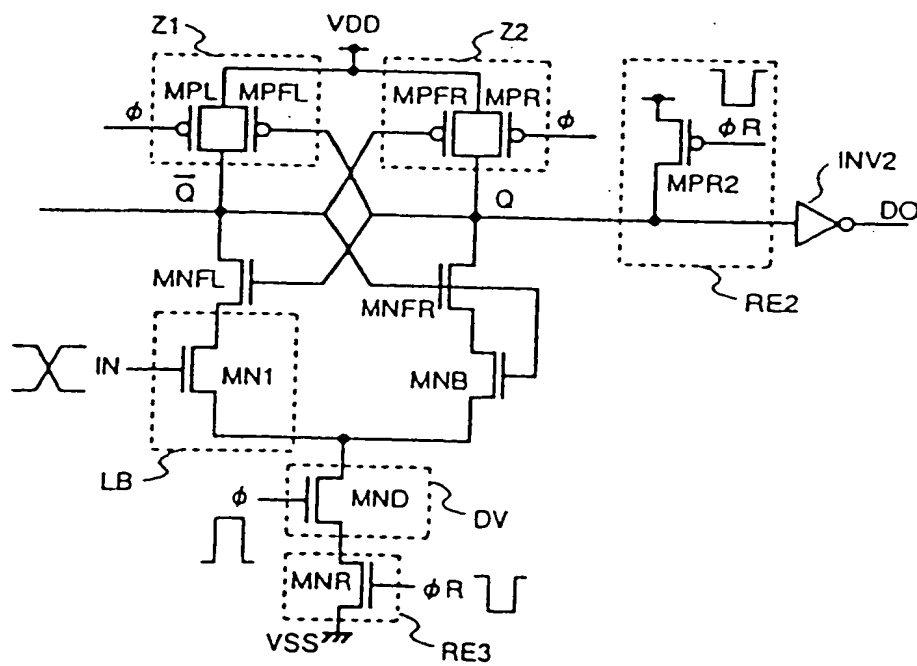


FIG. 33

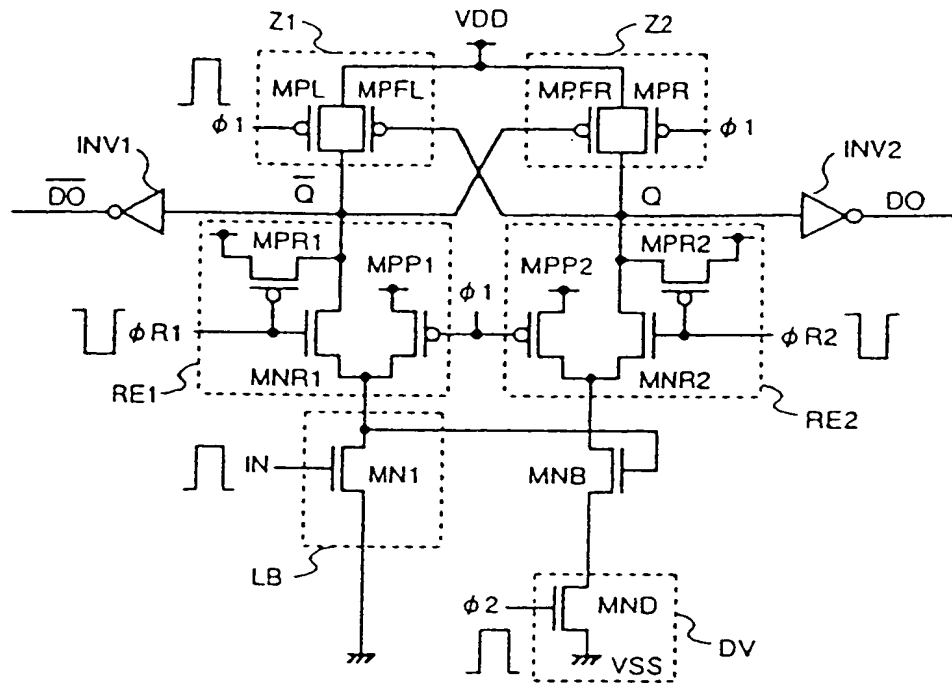


FIG. 34(a)

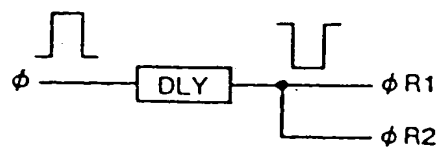


FIG. 34(b)

